IXYS

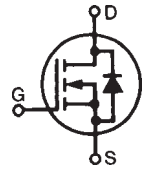
HiPerFET™ MOSFET
Q2-Class

IXFR 38N80Q2

V_{DSS} = 800 V
I_{D25} = 28 A
$R_{DS(on)}$ = 240 mΩ

$t_{rr} \leq 250$ ns

(Electrically Isolated Back Surface)

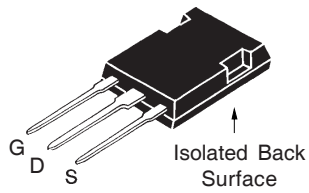


Preliminary Data Sheet

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	800	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	800	V
V_{GS}	Continuous	±30	V
V_{GSM}	Transient	±40	V
I_{D25}	T_C = 25°C	28	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	150	A
I_{AR}	T_C = 25°C	38	A
E_{AR}	T_C = 25°C	75	mJ
E_{AS}	T_C = 25°C	4.0	J
dv/dt	$I_S \leq I_{DM}$, di/dt ≤ 100 A/µs, $V_{DD} \leq V_{DSS}$, $T_J \leq$ 150°C, R_G = 2 Ω	20	V/ns
P_D	T_C = 25°C	416	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6 mm (0.063 in) from case for 10 s	300	°C
V_{ISOL}	50/60 Hz, RMS, t = 1 min	2500	V~
	I_{SOL} = 1mA, t = 1 s	3000	V~
F_C	Mounting Force		
Weight		5	g

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 3mA		800			V
$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 8 mA		2.0		4.5	V
I_{GSS}	V_{GS} = ±30 V_{DC}, V_{DS} = 0				±200	nA
I_{DSS}	V_{DS} = V_{DSS}	T_J = 25°C			50	µA
	V_{GS} = 0 V	T_J = 125°C			2	mA
$R_{DS(on)}$	V_{GS} = 10 V, I_D = I_T Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %				240	mΩ

ISOPLUS247 (IXFR)



G = Gate D = Drain
S = Source

Features

- Double metal process for low gate resistance
- Silicon chip on DCB substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- Epoxy meet UL 94 V-0, flammability classification
- Avalanche energy and current rated
- Fast intrinsic Rectifier

Advantages

- Easy assembly
- Space savings
- High power density

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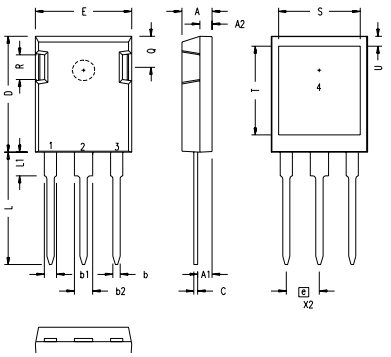
Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
g_{fs}	V_{DS} = 10 V; $I_D = I_T$, pulse test	25	37		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		8340		pF
C_{oss}			890		pF
C_{rss}			175		pF
$t_{d(on)}$	V_{GS} = 10 V, $V_{DS} = 0.5 \bullet V_{DSS}$, $I_D = I_T$		20		ns
t_r	R_G = 1.0 Ω (External),		16		ns
$t_{d(off)}$			60		ns
t_f			12		ns
$Q_{g(on)}$	V_{GS} = 10 V, $V_{DS} = 0.5 \bullet V_{DSS}$, $I_D = I_T$		190		nC
Q_{gs}			44		nC
Q_{gd}			88		nC
R_{thJC}				0.3	K/W
R_{thCK}			0.15		K/W

Source-Drain Diode — Characteristic Values (T_J = 25°C, unless otherwise specified)

Symbol	Test Conditions	min.	typ.	max.	
I_S	V_{GS} = 0 V			38	A
I_{SM}	Repetitive; pulse width limited by T_{JM}			150	A
V_{SD}	$I_F = I_S$, V_{GS} = 0 V, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %			1.5	V
t_{rr}	I_F = 25A, -di/dt = 100 A/µs, V_R = 100 V			250	ns
Q_{RM}			1		µC
I_{RM}			10		A

Notes: 1. Test current I_T = 19A
2. See IXFK38N80Q2 data sheet for characteristic curves

ISOPLUS247 Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 4,850,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463

Fig. 1. Output Characteristics @ 25ºC

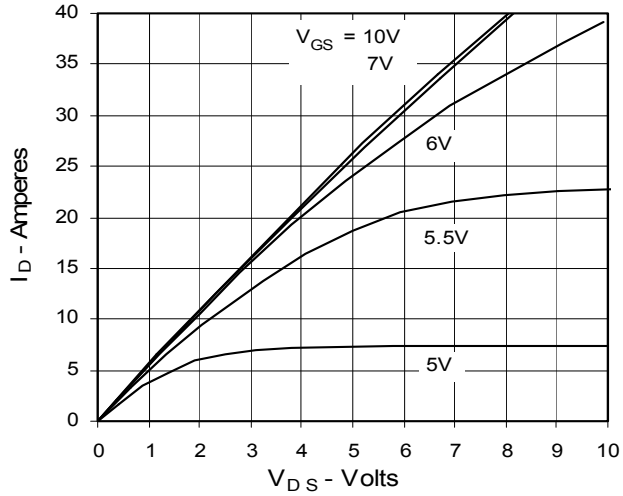


Fig. 2. Extended Output Characteristics @ 25ºC

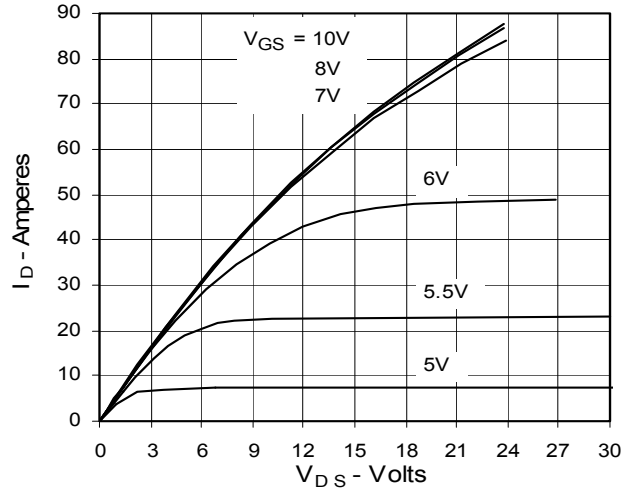


Fig. 3. Output Characteristics @ 125ºC

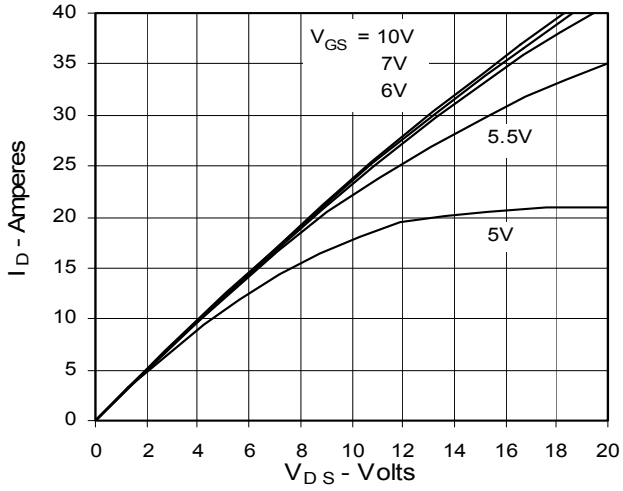


Fig. 4. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. Junction Temperature

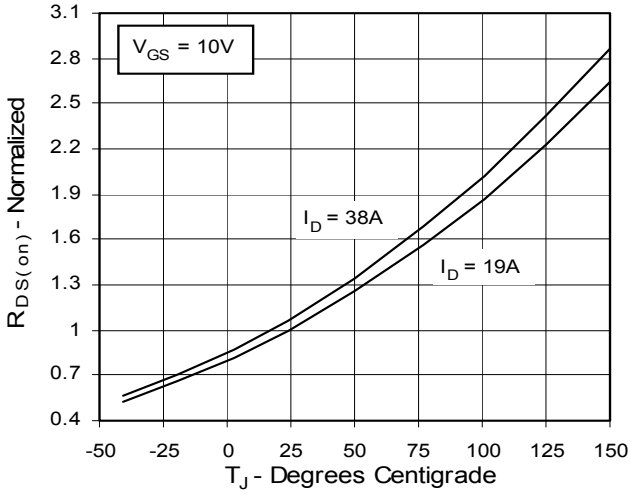


Fig. 5. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. I_D

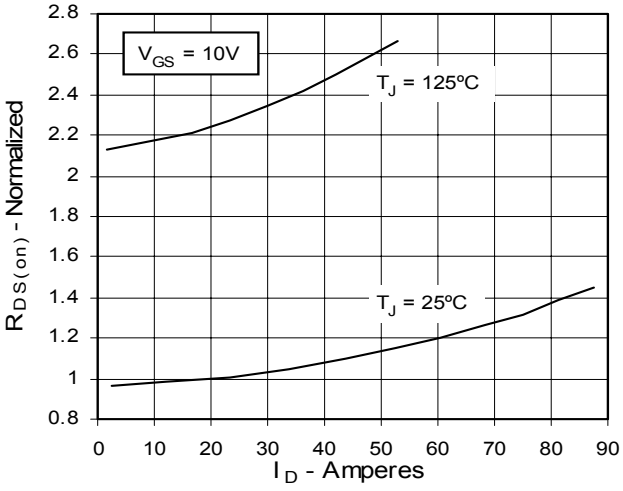


Fig. 6. Drain Current vs. Case Temperature

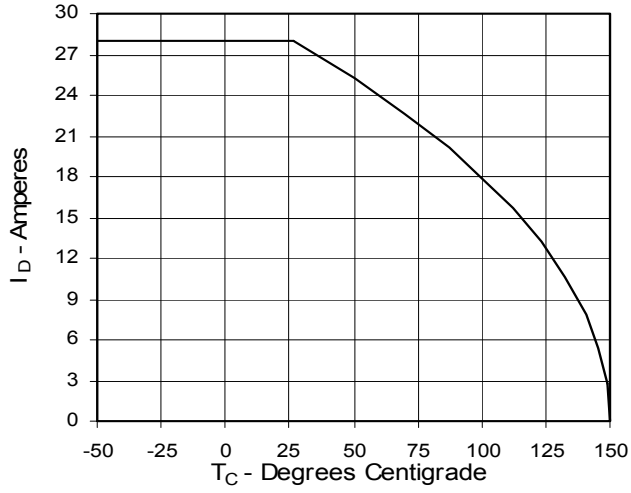


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Fig. 7. Input Admittance

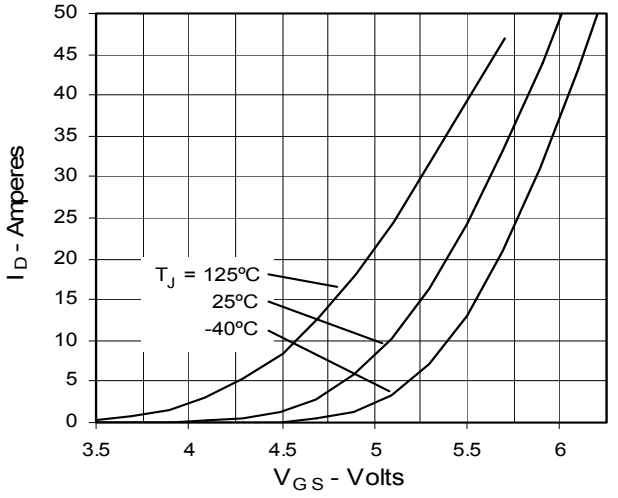

Fig. 8. Transconductance

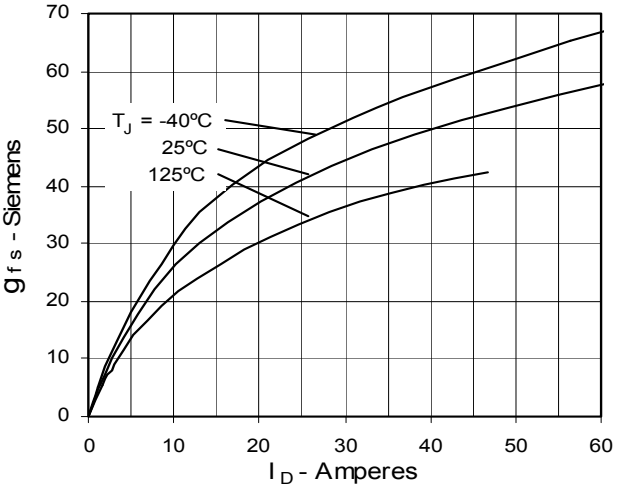

Fig. 9. Source Current vs. Source-To-Drain Voltage

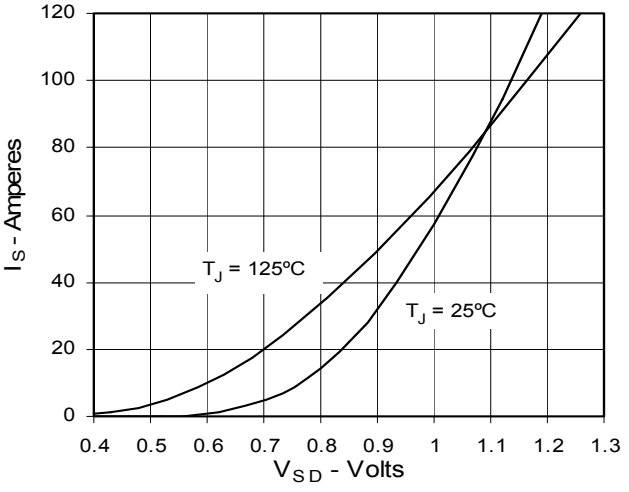

Fig. 10. Gate Charge

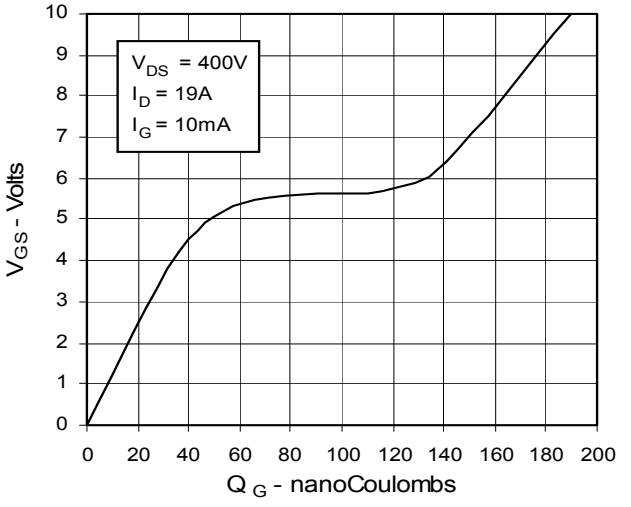

Fig. 11. Capacitance

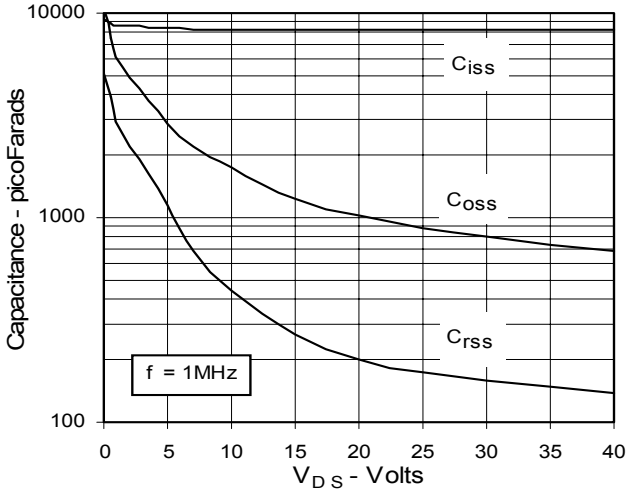

Fig. 12. Forward-Bias Safe Operating Area

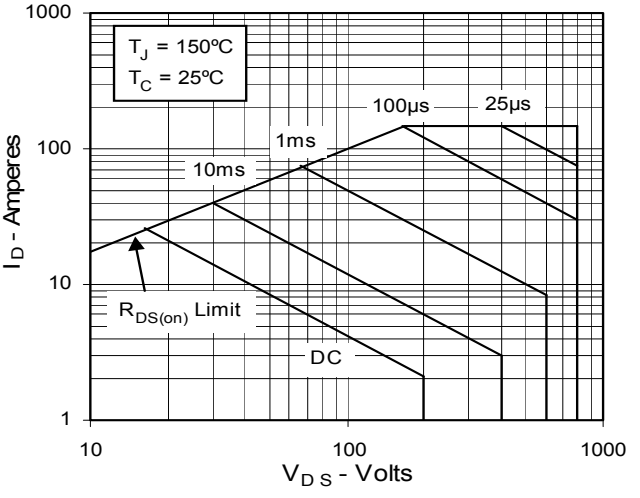

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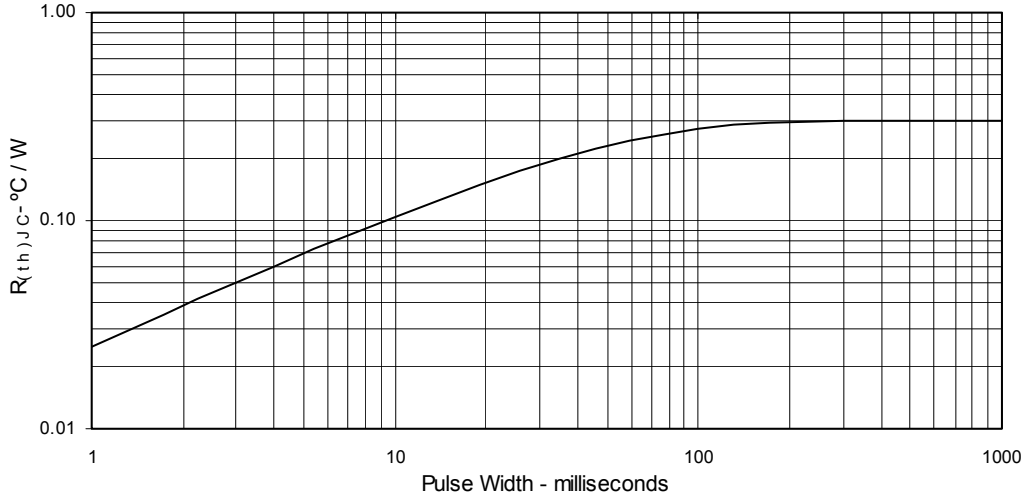
Fig. 13. Maximum Transient Thermal Resistance



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